16-Bit High Accuracy DAC

Features

- Full 16-Bit Performance
- 2.7-V – 5.5-V Single-Supply Operation
- High Accuracy: INL 1LSB
- Fast Settling Speed: 1 μs
- 10-nV/√Hz Output Noise Density
- Unbuffered Voltage Output
- SPI Compatible Interface
- Power-On Reset to 0 V (TPC2160 and TPC2161) or mid-scale (TPC2161M)
- Low Glitch: 10 nV-sec
- TPC2160 Package: SOP-8
- TPC2161/TPC2161M Package: SOP-14

Applications

- Data Acquisition Systems
- Automatic Test Equipment
- Industrial Process Control

Description

The TPC2160 and TPC2161/TPC2161M are single-channel, 16-bit, voltage output digital-to-analog converters with SPI interface. They accept a wide supply voltage range.

The TPC2160 output is 0 V to V_{REF}, and the TPC2161/ TPC2161M can provides bipolar output $\pm V_{REF}$ with external buffer and internal feedback resistor ladder.

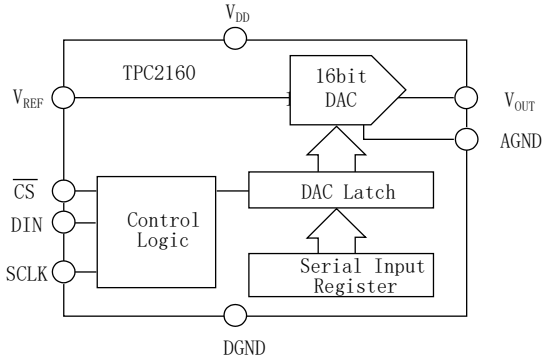
These parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0 V (TPC2160 and TPC2161), or mid-scale (TPC2161M).

The DACs provides 16-bit resolution over the full specified temperature range of −40 °C to 105 °C.

The DACs achieve a 1-μs settling time. The outputs are unbuffered, with low power consumption and low offset errors.

Providing a low noise performance of 10 nV/√Hz and low glitch, the DACs are suitable for deployment across multiple end systems.

Functional Block Diagrams



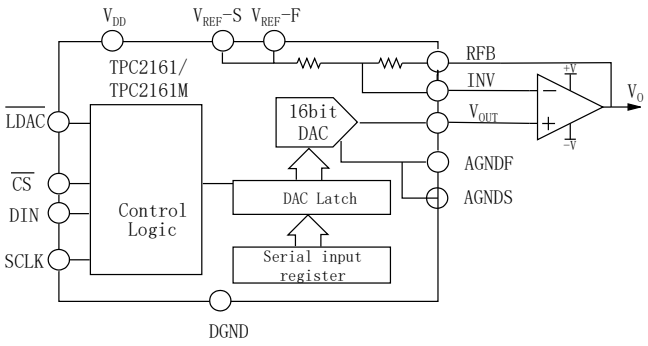


Table of Contents

Product Family Table

Order Number	Resolution	Reference	Output POR status	Package
TPC2160	16	External	0	SOP8
TPC2161	16	External	0	SOP14
TPC2161M	16	External	Midscal	SOP14

Revision History

Date	Revision	Notes
2021-06-16	Rev.A.1	Initial version
2021-08-24	Rev.A.2	Updated Absolute Maximum Ratings
2022-01-17	Rev.A.3	Updated reference input impedance
2022-12-27	Rev.A.4	Corrected TPC2161 name suffix
2023-04-03	Rev.A.5	Updated VIH/VIL threshold
2024-02-21	Rev.A.6	Added TPC2161M information

Pin Configuration and Functions

TPC2160
SOP8 Package
Top View

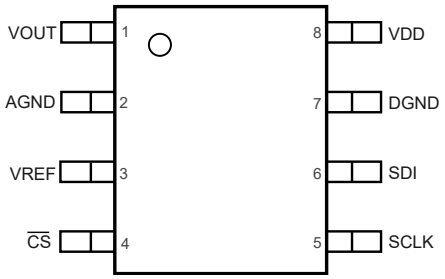


Table 1. Pin Functions: TPC2160

Pin No.	Pin Name	Description
1	V_{OUT}	DAC analog output
2	AGND	Analog Ground
3	V_{REF}	Voltage Reference Input for the DAC
4	$\overline{CS}$	Chip select input (active low)
5	SCLK	Clock Input. Data is clocked into the input register on the rising edge of SCLK
6	SDI	Serial Data Input
7	DGND	Digital Ground
8	V_{DD}	Analog Supply Voltage

TPC2161
SOP14 Package
Top View

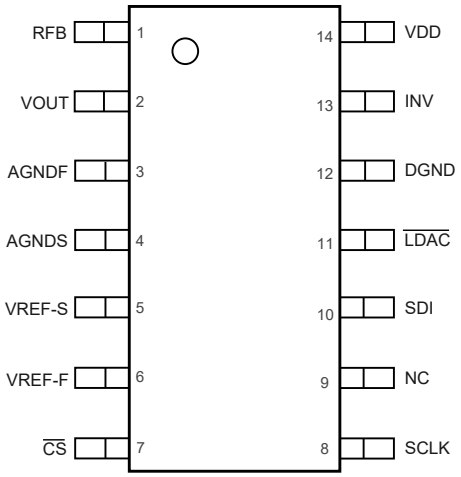


Table 2. Pin Functions:TPC2161

Pin No.	Pin Name	Description
1	RFB	Feedback resistor. Connect to the output of external operational amplifier in bipolar mode.
2	V_{OUT}	Analog output of DAC
3	AGNDF	Analog ground (Force)
4	AGNDS	Analog ground (Sense)
5	V_{REF} – S	Voltage reference input (Sense). Connect to external voltage reference.
6	V_{REF} – F	Voltage reference input (Force). Connect to external voltage reference.
7	$\overline{CS}$	Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low.
8	SCLK	Serial clock input
9	NC	No internal connection
10	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK
11	$\overline{LDAC}$	Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.
12	DGND	Digital ground
13	INV	Junction point of internal scaling resistors. Connect to external operational amplifier inverting input in bipolar mode.
14	V_{DD}	Analog power supply, +3 V to +5 V

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Typ	Max	Unit
Supply Voltage	$V^+ - V^-$	−0.3		6	V
	Analog Input Voltage	−0.3		$V^+ + 0.3$	V
	Digital Input Voltage to DGND	−0.3		$V^+ + 0.3$	V
	V_{OUT} to AGND	−0.3		$V^+ + 0.3$	V
	AGND, AGNDF, AGNDS to DGND	−0.3		+0.3	V
	Input Current: +IN, −IN (2)	−10		+10	mA
	Output Current: OUT	−10		+10	mA
	Operating Temperature Range	−40		125	℃
	Maximum Junction Temperature			150	℃
	Storage Temperature Range	−65		150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) The inputs are protected by ESD protection diodes to each power supply.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 (1)	5.5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 (2)	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD	Analog Supply Voltage	2.7		5.5	V
VIO	Digital IO Supply Voltage	1.7		5.5	V
Digital input voltage	Digital Input Voltage	0		VIO	V
VREFIN	Reference Divider Disabled	1.2		(VDD-0.2)/2	V
	Reference Divider Enabled	2.4		VDD-0.2	V
	Reference Divider Disabled	1.2		VDD/2	V
	Reference Divider Enabled	2.4		VDD	V
TJ	Operating Junction Temperature	–40		125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOP8	112.4	64.1	°C/W
SOP14	96.7	46.7	°C/W

Electrical Characteristics

All test conditions: V_{DD} = 2.7 V to 5.5 V, 2.5 V ≤ VREF ≤ V_{DD}, AGND = DGND = 0 V. All specifications TA = -40 to 105 ℃, unless otherwise noted.

Parameter	Test conditions	Min	Typ	Max	Unit
Static Performance					
Linearity Error				±1	LSB
Differential Linearity Error				±1	LSB
Gain Error			±0.5	±7	LSB
Gain Drift			±0.1		ppm/℃
Zero Code Error			±0.3	±2	LSB
Zero Code Drift			±0.05		ppm/℃
Output Characteristics					
Voltage Output		0		V_{DD}	V
Output Impedance			6.25		kΩ
Feedback Resistor (TPC2161)	RFB, RINV		28		kΩ
Bipolar Resistor Matching	RFB / RINV		1		Ω/Ω
	Ratio error		0.01		%
Dynamic Performance					
Settling Time	To 1/2 LSB of FS, CL = 10 pF		1		uS
Slew Rate	CL = 10 pF@5 V		25		V/μs
Digital-To-Analog Glitch	1 LSB change around major carry		10		nV-s
Digital Feedthrough			0.2		nV-s
Output Noise (TPC2160)	DAC code = 0x8400, frequency = 1 kHz TA = +25°C		10		nV/√Hz
Output Noise (TPC2161)	DAC code = 0x8400, frequency = 1 kHz TA = +25°C		18		nV/√Hz
Power-Supply Rejection	V_{DD} varies ±10%		±0.1		LSB
Reference Input (2)					
Reference Input Voltage Range		1.25		V_{DD}	V
Reference Input Impedance (1) (TPC2160)	Unipolar mode	8.5			kΩ
Reference Input Impedance (1) (TPC2161)	Unipolar mode	6.5			kΩ
Reference –3dB Bandwidth, BW	Code = FFFFh		1.3		MHz
Reference Feedthrough	Code = 0000h, VREF = 1 VPP at 100 kHz		1		mV

Electrical Characteristics (continued)

All test conditions: V_{DD} = 2.7 V to 5.5 V, 2.5 V ≤ VREF ≤ V_{DD}, AGND = DGND = 0 V. All specifications TA = -40 to 105 ℃, unless otherwise noted.

Parameter	Test conditions	Min	Typ	Max	Unit
Reference Input (2)					
Signal-to-Noise Ratio, SNR			92		dB
Reference Input Capacitance	Code = 0000h		75		pF
	Code = FFFFh		120		pF
Digital Inputs					
VIL Input Low Voltage	V_{DD} = 2.7 V			0.6	V
	V_{DD} = 5 V			0.8	
VIH Input High Voltage	V_{DD} = 2.7 V	2.1			V
	V_{DD} = 5 V	2.4			
Input Current			±0.5	5	μA
Input Capacitance (2)				10	pF
Hysteresis Voltage (2)			0.4		V
Power Supply					
V_{DD} Power-Supply Voltage		2.7		5.5	V
I_{DD} Power-Supply Current	V_{DD} = 5			150	μA
Power	V_{DD} = 5			825	μW
SPI					
Fclk				25	MHz

(1) Reference input resistance is code-dependent, minimum at 0x8555.
(2) Guaranteed by design, not subject to production test.

Timing Characteristics

All test conditions are: V_{DD} = 2.7 V to 5.5 V ±10%, VREF = 2.5 V, VINH = 3 V and 90% of V_{DD}, VINL = 0 V and 10% of V_{DD}, AGND = DGND = 0 V; TA = -40 to 105 ℃, unless otherwise noted.

Parameter (1) (2)	Limit	Unit	Description
f_{SCLK}	25	MHz max	SCLK cycle frequency
t_1	40	ns min	SCLK cycle time
t_2	20	ns min	SCLK high time
t_3	20	ns min	SCLK low time
t_4	10	ns min	$\overline{CS}$ low to SCLK high setup
t_5	15	ns min	$\overline{CS}$ high to SCLK high setup
t_6	30	ns min	SCLK high to $\overline{CS}$ low hold time
t_7	20	ns min	SCLK high to $\overline{CS}$ high hold time
t_8	15	ns min	Data setup time
t_9	4	ns min	Data hold time (VINH = 90% of V_{DD}, VINL = 10% of V_{DD})
t_{10}	7.5	ns min	Data hold time (VINH = 3V, VINL = 0 V)
t_{11}	30	ns min	$\overline{LDAC}$ pulse width
t_{12}	30	ns min	$\overline{CS}$ high to $\overline{LDAC}$ low setup

(1) Guaranteed by design and characterization. Not production tested.
(2) All input signals are specified with $t_R = t_F$ = 1 ns/V and timed from a voltage level of (V_{INL}+ V_{INH})/2.

Timing Diagrams

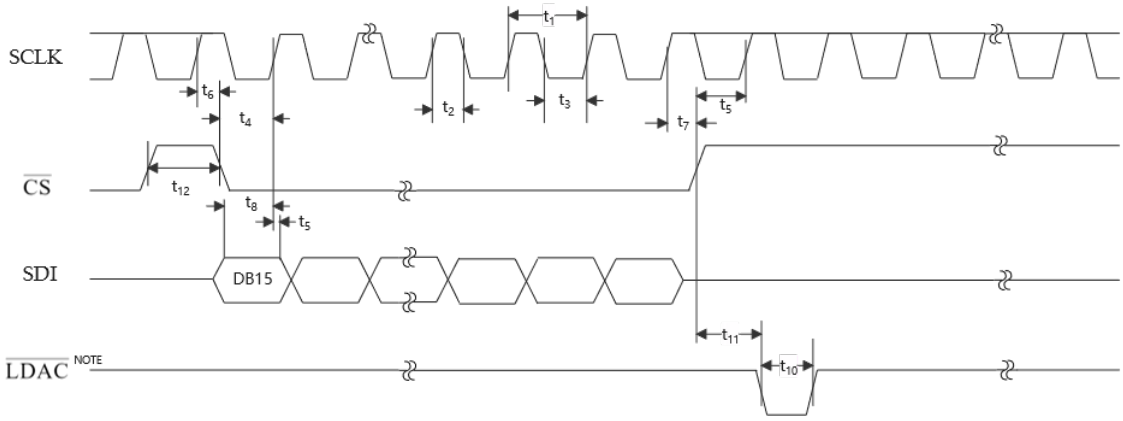


Figure 1. SPI Timing Diagram

Note:

TPC2161 ONLY. Can be tied permanently low if required.

Typical Performance Characteristics

All test conditions are: TA = 25°C, VDD = 5.5 V, Internal Reference = 2.5 V, Gain = 2, DAC outputs unloaded, unless otherwise noted.

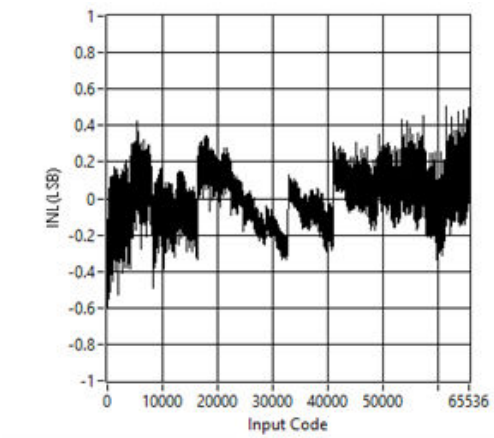


Figure 2. INL

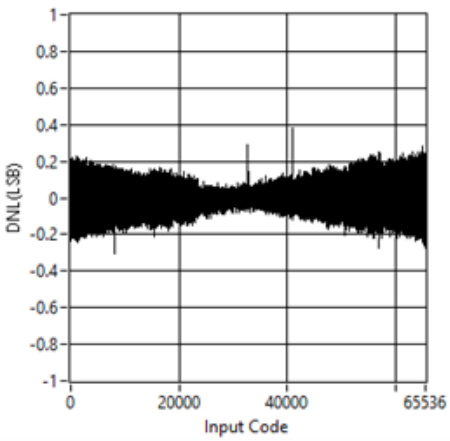


Figure 3. DNL

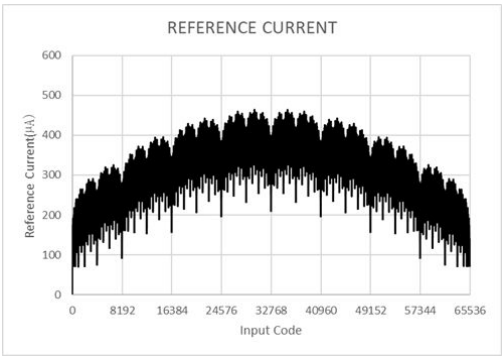


Figure 4. Reference Current

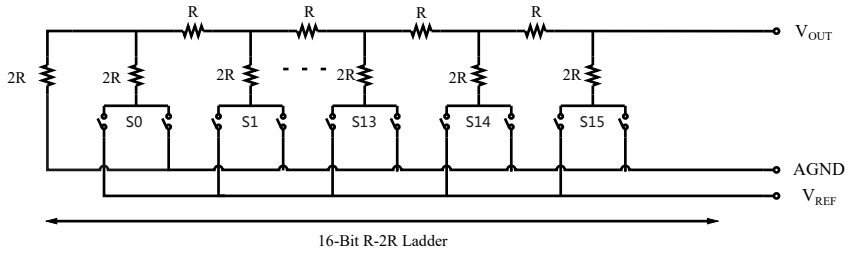
Detailed Description

Overview

The TPC2160 and TPC2161 are single-channel, 16-bit, DACs with R-2R structure. They have an SPI serial interface, with 16-bit word format. The TPC2160 and TPC2161 are reset to zero code.

Ditigal-to-Analog Sections

A simplified DAC diagram is shown below. The 16 bits of the data word drive switches S0 to S15 of a 16-bit voltage mode R-2R ladder network.



Feature Description

Output Range

The output of the DAC is:

$$V_{OUT} = (V_{REF} \times Code)/65536 \quad (1)$$

Where *Code* is the decimal data word loaded to the DAC latch.

Power-On Reset

The devices have power-on reset function, to make sure the output is a known state at power-up, and the DAC Registers are zero (TPC2160 and TPC2161) or mid-scale(TPC2161M) until new data are loaded. Therefore, after power-up, the output of V_{OUT} is 0 V (TPC2160 and TPC2161), or mid-scale(TPC2161M).

Serial Interface

The digital interface is a standard 3-wire serial interface compatible with SPI.

When $\overline{CS}$ turns low, the transmission is started, and the SDI data is shifted in and latched on the edge of SCLK. The data registers are 16-bit, so $\overline{CS}$ must go high after 16 SCLKs transfers a whole data word.

For the TPC2160, the input register is latched to DAC immediately after the input register is loaded, so the DAC output is updated at the same time.

The TPC2161 has an $\overline{LDAC}$ pin. After $\overline{CS}$ goes high, the DAC register can be updated by bringing $\overline{LDAC}$ low. $\overline{LDAC}$ can also be tied low permanently. In this case, the DAC register is updated immediately after the input register is loaded, and DAC output is updated at the same time.

TPC2160 Unipolar Output Operation

DAC Latch Contents		
MSB	**LSB**	**Analog Input**
1111 1111 1111 1111		V_{REF} × (65,535 / 65,536)
1000 0000 0000 0000		V_{REF} × (32,768 / 65,536) = ½ V_{REF}
0000 0000 0000 0001		V_{REF} × (1 / 65,536)
0000 0000 0000 0000		0 V

Considering gain error, INL and zero-scale error, the worst-case output voltage can be calculated by the following equation:

Unipolar Mode Worst-Case Output

$$V_{OUT\_U} = \frac{D}{2^{16}} \times (V_{REF} + V_{GE}) + V_{ZSE} + INL \quad (2)$$

Where:

V_{OUT_U} = Unipolar mode worst-case output

D = Code loaded to DAC

V_{REF} = Reference voltage

V_{GE} = Gain error in volts

V_{ZSE} = Zero-scale error in volts

INL = Integral nonlinearity in volts

TPC2161 Bipolar Output Operation

DAC Latch Contents		
MSB	**LSB**	**Analog Input**
1111 1111 1111 1111		$+V_{REF} \times (32{,}767 / 32{,}768)$
1000 0000 0000 0001		$+V_{REF} \times (1 / 32{,}768)$
1000 0000 0000 0000		0 V
0111 1111 1111 1111		$-V_{REF} \times (1 / 32{,}768)$
0000 0000 0000 0000		$-V_{REF} \times (32{,}768 / 32{,}768) = -V_{REF}$

Considering non-idealities of external amplifier, the worst-case output voltage can be calculated from the following equation:

Bipolar Mode Worst-Case Output

$$V_{OUT\_B} = \frac{\left[\left(V_{OUT\_U} + V_{OS}\right)(2 + RE) - V_{REF}(1 + RE)\right]}{1 + \frac{2 + RE}{A}} \quad (3)$$

Where:

V_{OS} = External operational amplifier input offset voltage

RE = RFB and RIN resistor matching error

A = Operational amplifier open-loop gain

Output Amplifier Selection

For bipolar mode, to provide the $\pm V_{REF}$ output, a precision amplifier should be used, supplied from a dual power supply.

In a single-supply application, selection of a suitable operational amplifier is also important. Input offset, input bias current, rail-to-rail input, and output range, −3dB bandwidth and slew rate, are key features for amplifier selection.

Power Supply and Reference Bypassing

It is recommended that the reference and supply pins are bypassed with a 10-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor, for good supply and noise suppression, and then accurate performance

Application and Implementation

> Note
>
> Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

Multiple Devices Decoding

The $\overline{CS}$ pin of the device can be used to select one of muitiple DACs. All devices can share and receive the same serial clock and serial data, but only one device receives the $\overline{CS}$ signal at any one time.

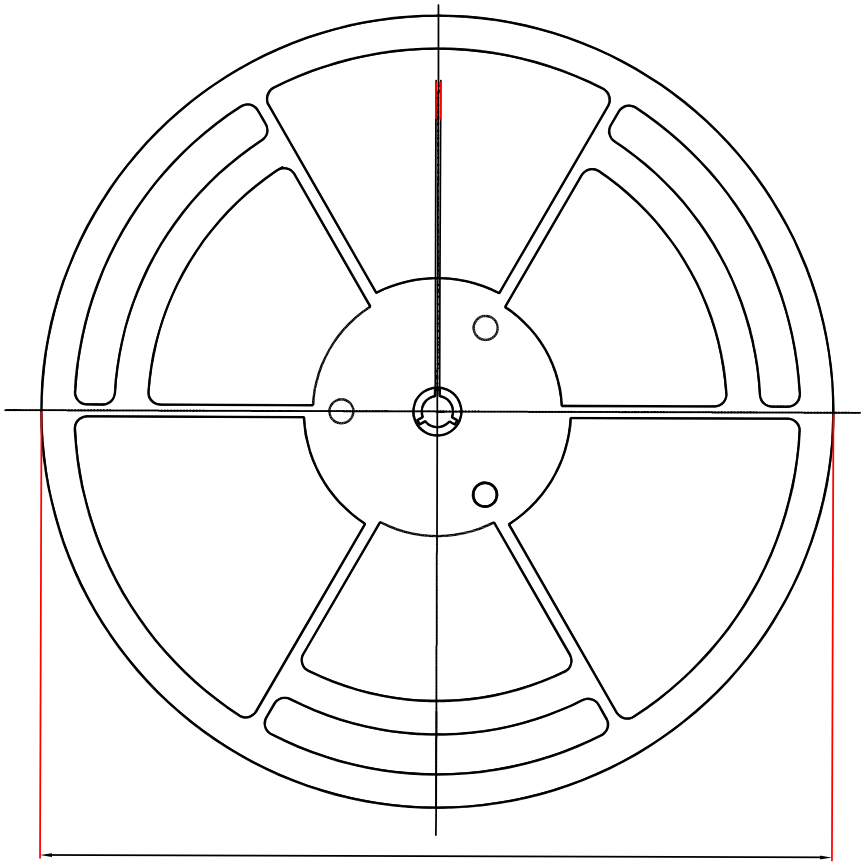
Layout

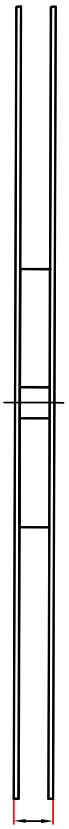
Layout Guideline

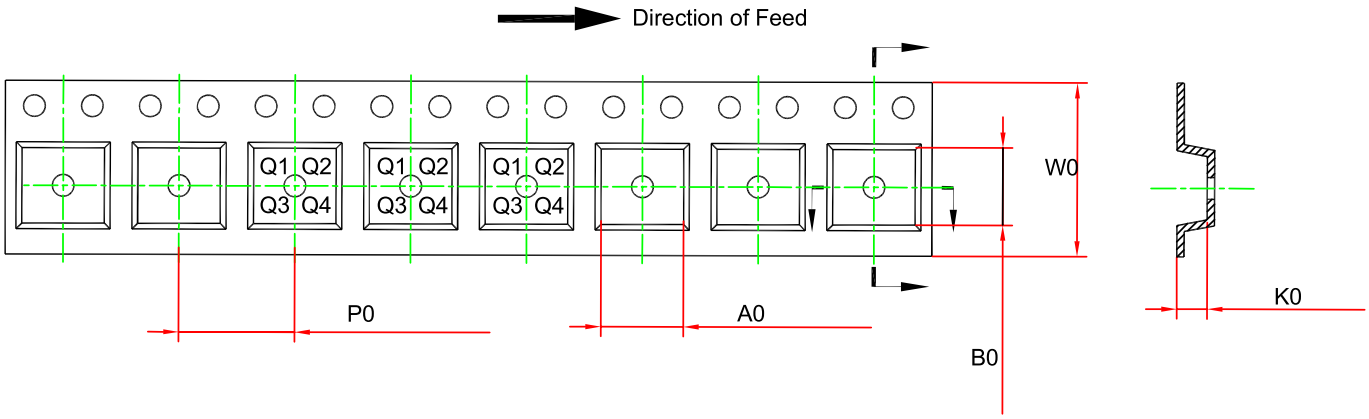
When designing the PCB for high performance circuit, power supply and grounding layout should be carefully considered. Ensure that the analog and digital sections are clearly separated. If multiple devices require an analog ground connection to the digital ground, establish a single point of connection. Put the device close to star ground point as close as possible.

Additionally, the device should have adequate bypass capacitors of 10 μF in parallel with 0.1 μF capacitors, placed as close to the package as feasible, ideally adjacent to the device. The 10 μF capacitors should be of the tantalum bead type, while the 0.1 μF capacitors should exhibit low effective series resistance (ESR) and inductance (ESI), similar to ceramic capacitors, providing a low-impedance path to ground at high frequencies to handle transient currents resulting from internal logic switching.

Tape and Reel Information







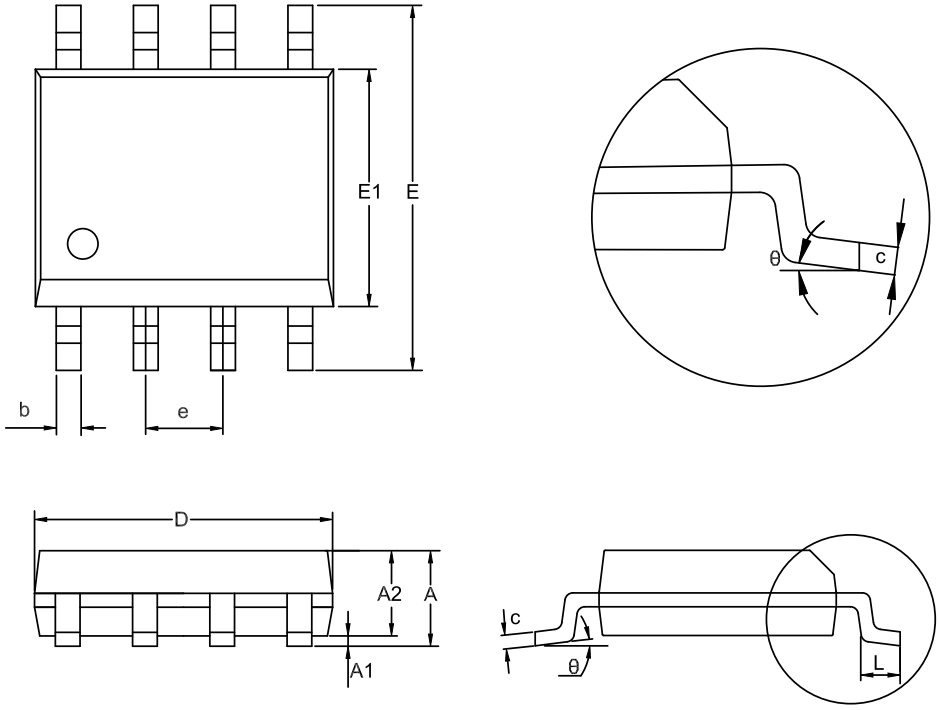
Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC2160S1L1 A-SO1R-S	SOP8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1

Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPC2161S1L1-SO2R	SOP14	330.0	21.6	6.5	9.5	2.3	8.0	16.0	Q1
TPC2161MS1L1-SO2R	SOP14	330.0	21.6	6.5	9.5	2.3	8.0	16.0	Q1

Package Outline Dimensions

SOP8

Package Outline Dimensions SO1(SOP-8-A)



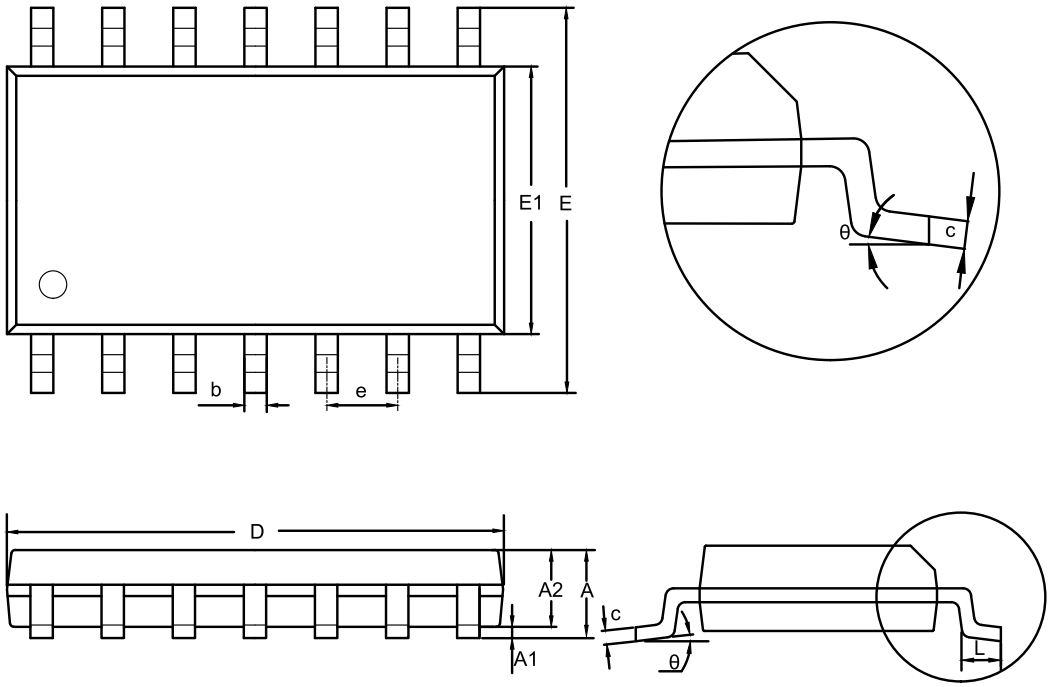
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

SOP14

Package Outline Dimensions SO2(SOP-14-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPC2160S1L1A-SO1R-S	−40 to 125°C	SOP8	2160	1	Tape and Reel, 4000	Green
TPC2161S1L1-SO2R	−40 to 125°C	SOP14	2161	1	Tape and Reel, 2500	Green
TPC2161MS1L1-SO2R	−40 to 125°C	SOP14	2161M	1	Tape and Reel, 2500	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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